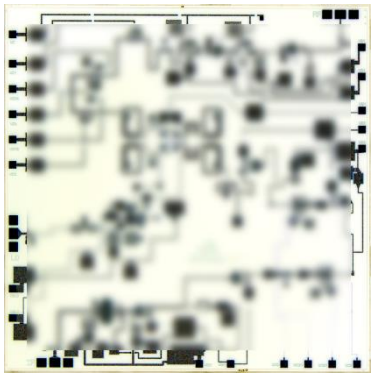
MECKuSCFC

Ku-to-Ku Single Chip Frequency Converter



Product Description

MECKuSCFC is a Ku-to-Ku band full frequency high-linearity downconverter. It is based on a 0.15 µm GaAs pHEMT space evaluated process.

The MECKuSCFC integrates in a single MMIC up to 8 different operating blocks to provide, in addition to the frequency conversion, programmable Gain control, compensation of gain variation over temperature, RF, IF and LO signals amplification.

In the IF frequency band [10.7 – 12.7] GHz, synthesized by LO frequencies in the range [1.5 – 3.3] GHz and RF frequency in the band [13.0 – 14.5] GHz, the MECKuSCFC offers a conversion gain of about 47 dB, an output power of 24 dBm at 1 dB of gain compression and an output TOI of 33 dBm. A 20 dB programmable gain attenuation, with 1 dB steps, and a continuous 5 dB fine tuning, to fully compensate the gain variation over temperature, are also integrated in the chip.

It is available in a 5x5 mm^2 bare die.

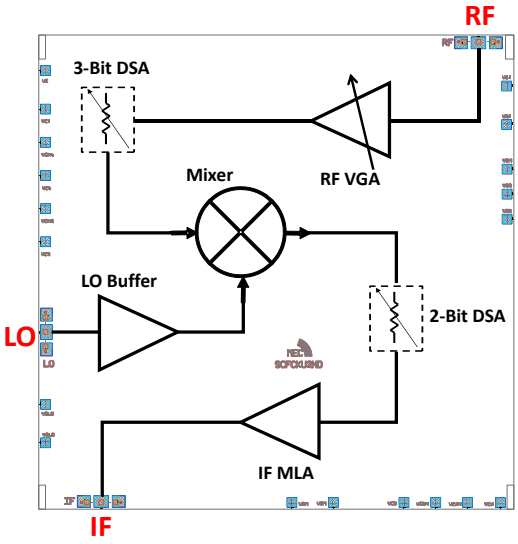
Applications

Telecom Satellite Applications

Main Features

- 0.15µm GaAs pHEMT space evaluated process
- Full performance in the frequency bands:
  - RF: 13.0 – 14.5 GHz
  - LO: 1.5 – 3.3 GHz
  - IF: 10.7 – 12.7 GHz
- +27 to +47 dB minimum Conversion Gain
- 20 dB Gain variation 1 dB step
- 5 dB of continuous Gain variation for temperature compensation
- Maximum Linear operating Output Power from 2 to 9 dBm
- C/I3 higher than 50 dBc at 9 dBm of output power
- Power consumption of 1 W
- Fixed Bias: VDD = 4.5 V, Idq = 217 mA
- 9 control signals (-1.5 V; 0 V) to implement the 20 dB Gain variation 1 dB step
- Control voltage VC in the range [-4 – 0] V to perform the compensation over temperature
- Fully matched to 50 Ω, with integrated RF to DC decoupling
- Chip Size: 5.0 x 5.0 x 0.07 mm^3

Functional Block Diagram



Nominal Operating Conditions

Parameter	Min	Typ.	Max	Units
Temperature Range	-20	+30	+70	°C
VG1		-0.7		V
VD1		4.5		V
ID1q		27		mA
VGMx		-1.2		
VGLO		-0.5		V
VDLO		4.5		V
IDLOq		39		mA
VG2		-0.7		V
VD2		4.5		V
ID2q		58.5		mA
VGM		-0.7		V
VDM		4.5		V
IDMq		93		mA
VC	-4	-2.2	0	V
VC1	-1.5	*	0	V
VC2	-1.5	*	0	V
VC2N	-1.5	*	0	V
VC4	-1.5	*	0	V
VC4N	-1.5	*	0	V
VC5	-1.5	*	0	V
VC5N	-1.5	*	0	V
VC8	-1.5	*	0	V
VC8N	-1.5	*	0	V
PLO	2	4	6	dBm
PDC		1		W

- When operates under these recommended conditions, the device is compliant with ESA space-derating rules.
- Electrical specifications are measured at specified test conditions.
- The continuous Gain variation features can be achieved by applying a continuous variation to VC.
- The 20 dB Gain variation/attenuation, 1-dB step, can be implemented according to the following Control Table

Gain Control Table

Att	VC1	VC2	VC2N	VC4	VC4N	VC5	VC5N	VC8	VC8N
dB	*V*	*V*	*V*	*V*	*V*	*V*	*V*	*V*	*V*
0	0	0	-1.5	0	-1.5	0	-1.5	0	-1.5
1	-1.5	0	-1.5	0	-1.5	0	-1.5	0	-1.5
2	0	-1.5	0	0	-1.5	0	-1.5	0	-1.5
3	-1.5	-1.5	0	0	-1.5	0	-1.5	0	-1.5
4	0	0	-1.5	-1.5	0	0	-1.5	0	-1.5
5	-1.5	0	-1.5	-1.5	0	0	-1.5	0	-1.5
6	0	-1.5	0	-1.5	0	0	-1.5	0	-1.5
7	-1.5	-1.5	0	-1.5	0	0	-1.5	0	-1.5
8	-1.5	-1.5	0	0	-1.5	-1.5	0	0	-1.5
9	0	0	-1.5	-1.5	0	-1.5	0	0	-1.5
10	-1.5	0	-1.5	-1.5	0	-1.5	0	0	-1.5
11	0	-1.5	0	-1.5	0	-1.5	0	0	-1.5
12	-1.5	-1.5	0	-1.5	0	-1.5	0	0	-1.5
13	0	0	-1.5	0	-1.5	-1.5	0	-1.5	0
14	-1.5	0	-1.5	0	-1.5	-1.5	0	-1.5	0
15	0	-1.5	0	0	-1.5	-1.5	0	-1.5	0
16	-1.5	-1.5	0	0	-1.5	-1.5	0	-1.5	0
17	0	0	-1.5	-1.5	0	-1.5	0	-1.5	0
18	-1.5	0	-1.5	-1.5	0	-1.5	0	-1.5	0
19	0	-1.5	0	-1.5	0	-1.5	0	-1.5	0
20	-1.5	-1.5	0	-1.5	0	-1.5	0	-1.5	0

Absolute Maximum Rating

Parameter	Rating
VD	8 V
VG / VC	-2.5 to 0 V
Channel temperature, T_J	175 °C
PDC (T = 85 °C; VD = 4V)	1.5 W
RF Input Power	-8 dBm
LO Input Power	8 dBm
Mounting Temperature (<30 sec)	260 °C
Storage Temperature	-55 to +150 °C

These parameters are carried out from stress test analysis and foundry data.

Thermal and Reliability Information

Conditions	Parameter	Value
Nominal Bias Tbase = +70 °C - Pdiss = 0.98 W	Equivalent Thermal Resistance	47 °C/W
	Channel Temperature	116 °C
	Mean Time Failure	**> 2E+7 hrs**

Electrical Characteristics

Test conditions unless otherwise noted: Tbase = 30°C; Bias, typical values in previous table.

Parameter	Min.	Typ	Max	Units
Input Frequency Range (RF)	13.0		14.5	GHz
Output Frequency Range (IF)	10.7		12.7	GHz
LO Frequency Range (LO)	1.5		3.3	GHz
Operating RF Input levels	-55		-25	dBm
Overdrive survivability at RF port			-4	dBm
LO Input Power Range	2	4	6	dBm
Conversion Gain	27.5		47.5	dB
Gain Step		1		dB
Gain Stability				
Over any 15°C		0.1		dBpp
Over acceptance temp. range		1		dBpp
Over life (Excluding temperature effects)		0.7		dBpp
Gain Flatness				
Over any 500 MHz		0.25		dBpp
Over operational range		0.9		dBpp
Gain Slope		0.01		dB/MHz
Noise Figure				
Max Gain		6		dB
Min Gain		12		dB
Output P1dB				
Max Gain		+23		dBm
Min Gain		+22		dBm
Output IP3 level				
Max Gain	+33		+37	dBc
Min Gain	+29		+32	dBc
Amplitude Linearity - C/I3				
Max Gain (@ Pout = +9 dBm)	49.5		55.0	dBc
Min Gain (@ Pout = +2 dBm)	53.0		58.0	dBc
Single Carrier Spurious				
In-Band Spurious		-72 (1)		dBc
Out of Band Spurious		-22 (2)		dBc
LO harmonics attenuation		30		dBc
Output Return Loss	10			dB
Input Return Loss	10			dB
Power Consumption			1	W

(1) For specific frequency schemes
(2) 2.3 GHz below the IF band

Test Conditions

Test conditions unless otherwise noted: Tbase = 30°C, (VD1, VDLO, VD2, VDM) = 4.5 V, ID1q = 27 mA, IDLOq = 39 mA, ID2q = 58.5 mA, IDMq = 93 mA, VC (nominal) = -2.2 V, P_LO = 4 dBm. Control Voltages for Gain Variation applied as per "Gain Control Table". P_RF as per table below.

Gain & Power variation scheme

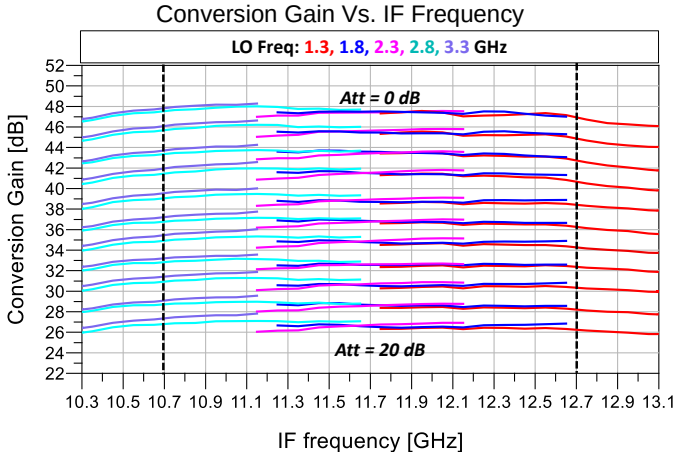
Reference Gain	*47*	*46*	*45*	*44*	*43*	*42*	*41*	*40*	*39*	*38*	*37*	*36*	*35*	*34*	*33*	*32*	*31*	*30*	*29*	*28*	*27*	*dB*
Input Level	-38	-37	-36	-35	-34	-33	-32	-31	-30	-29	-28	-27	-26	-25	-25	-25	-25	-25	-25	-25	-25	dBm
DSA Att.	0	-1	-2	-3	-4	-5	-6	-7	-8	-9	-10	-11	-12	-13	-14	-15	-16	-17	-18	-19	-20	dB
Nominal Pout	9	9	9	9	9	9	9	9	9	9	9	9	9	9	8	7	6	5	4	3	2	dBm

Adopted Conversion Scheme

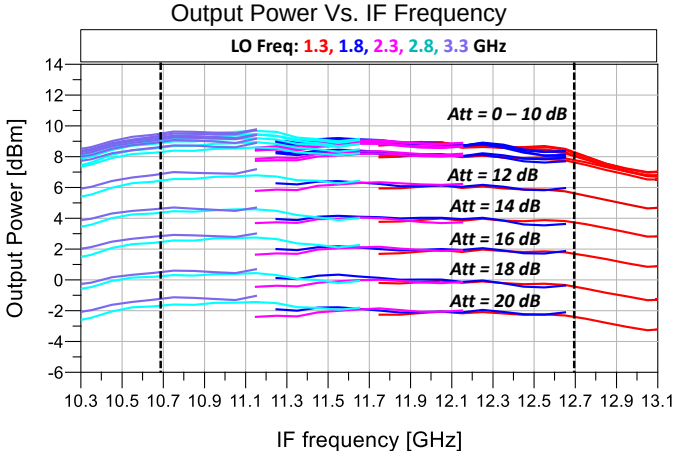
LO freq	1.3	1.8	2.3	2.8	3.3	GHz
Syn. #	1	2	3	4	5	
RF freq	IF freq.					
13.0	11.7	11.2	10.7	10.2	9.7	
13.5	12.2	11.7	11.2	10.7	10.2	
14.0	12.7	12.2	11.7	11.2	10.7	
14.5	13.2	12.7	12.2	11.7	11.2	
GHz	GHz	GHz	GHz	GHz	GHz	

Main Performance – Conversion Gain and Output Power

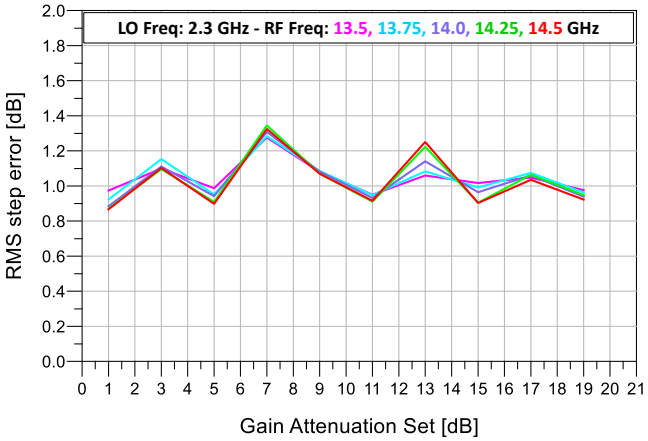
Conversion Gain Vs. IF Frequency



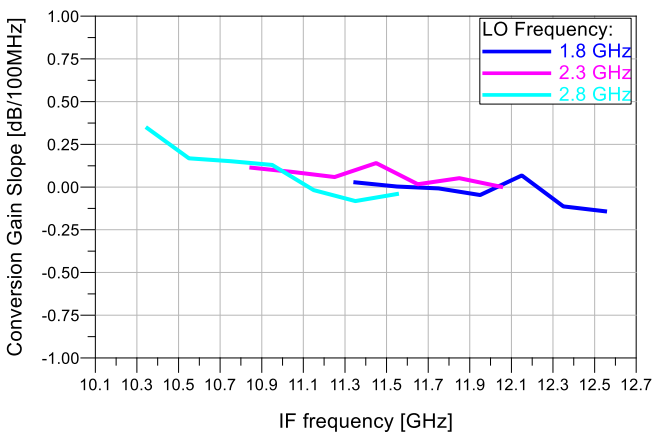
Output Power Vs. IF Frequency



Gain varition step error

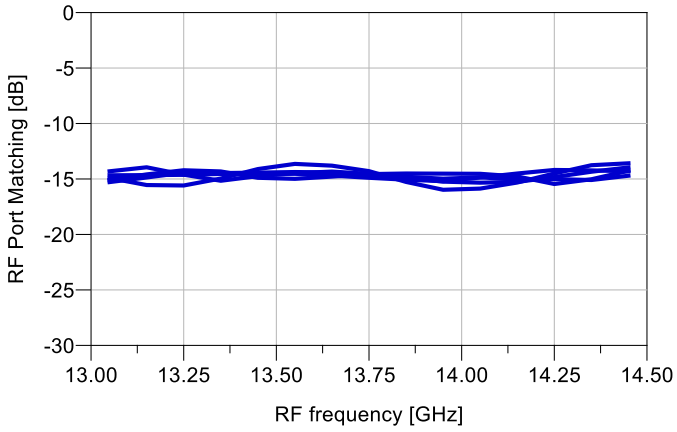


Output Power Vs. IF Frequency

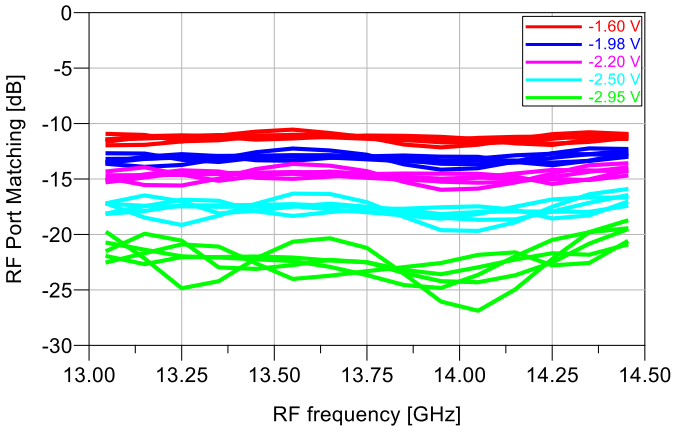


Main Performance – Port Matching

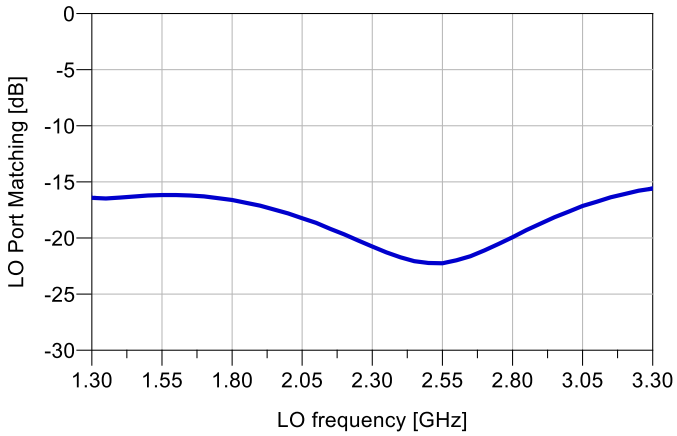
Return Loss @ RF Input port



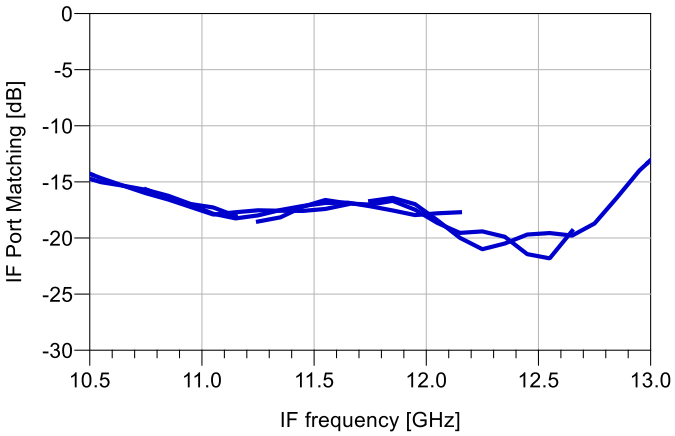
Return Loss @ RF input port Vs. Vc



Return Loss @ LO port



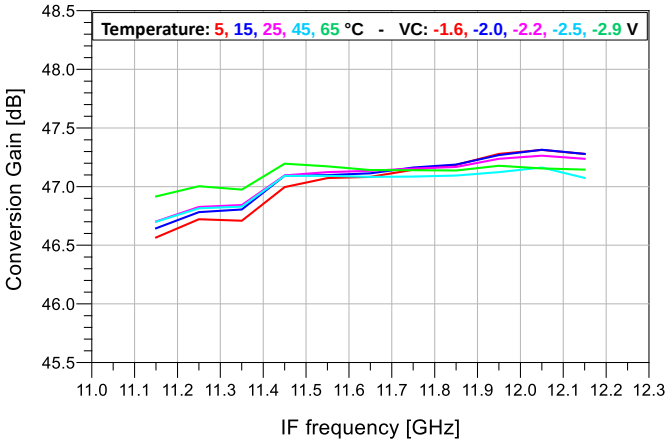
Return Loss @ IF output port



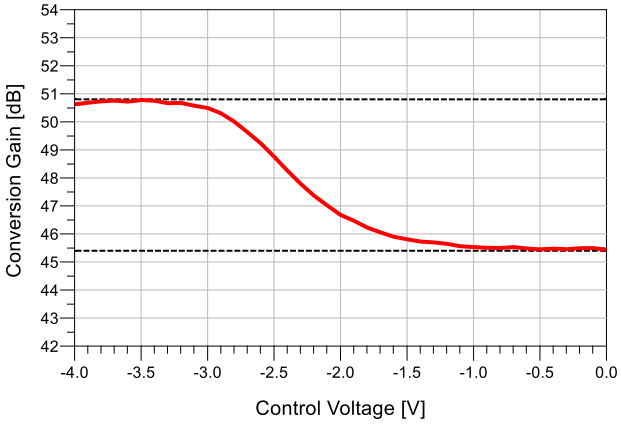
Main Performance – Conversion Gain Vs. Temperature

FLO = 2.3 GHz, FRF = [13.5 – 14.5] GHz, Attenuation = 0 dB

Conversion Gain Vs. IF Frequency

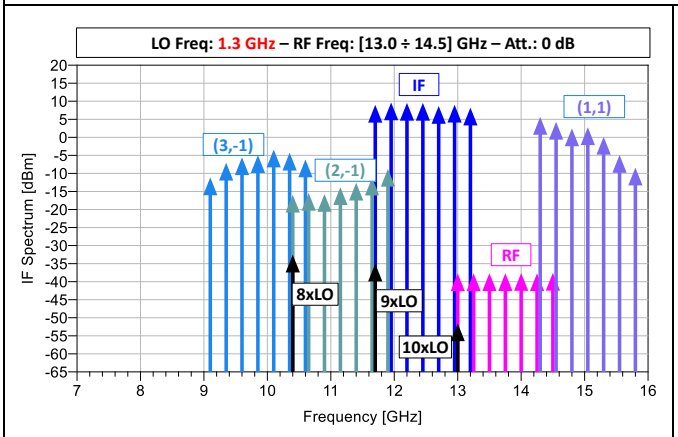


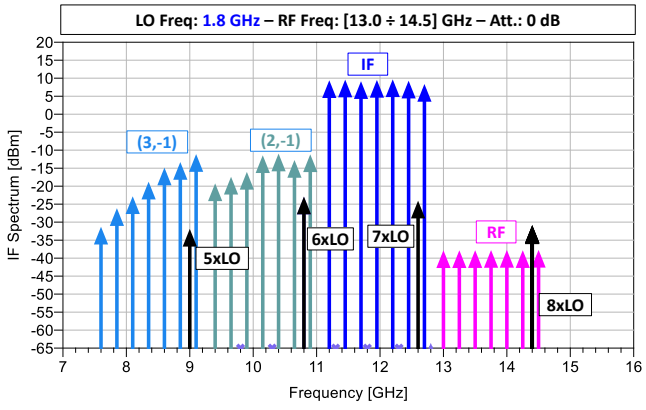
Output Power Vs. IF Frequency

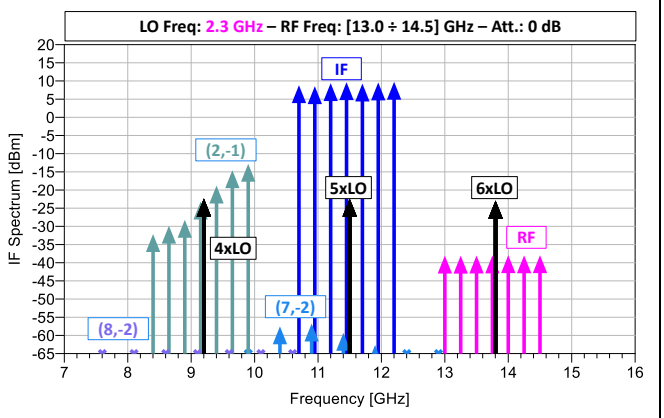


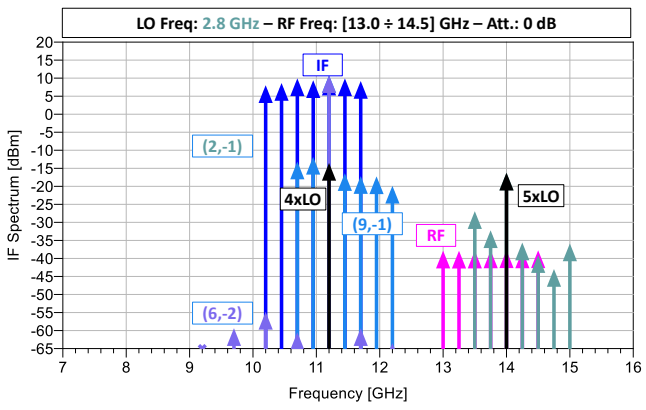
Main Performance – Output Spectrum

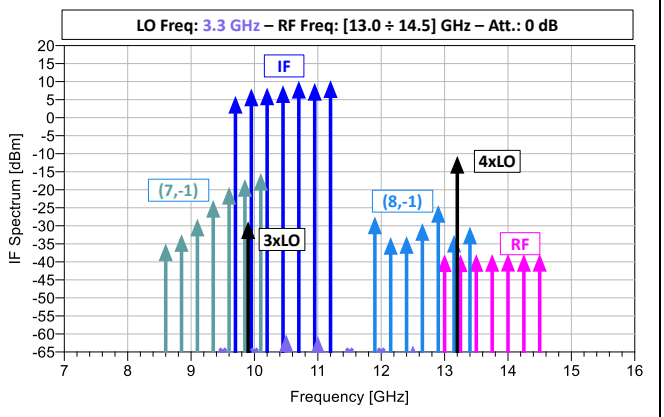
FRF = [13.0 – 14.5] GHz, Attenuation = 0 dB, VC = -2.2 V







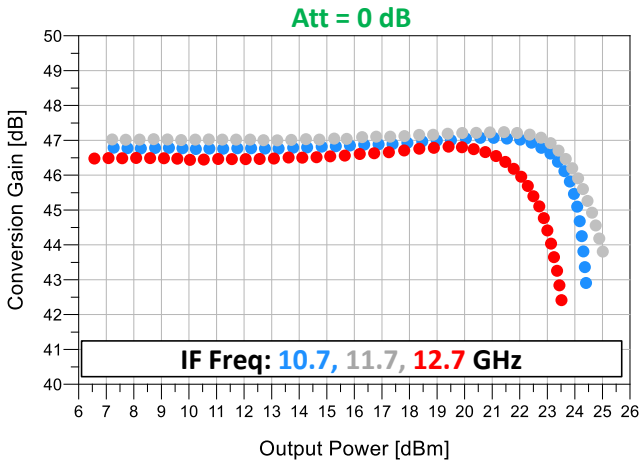


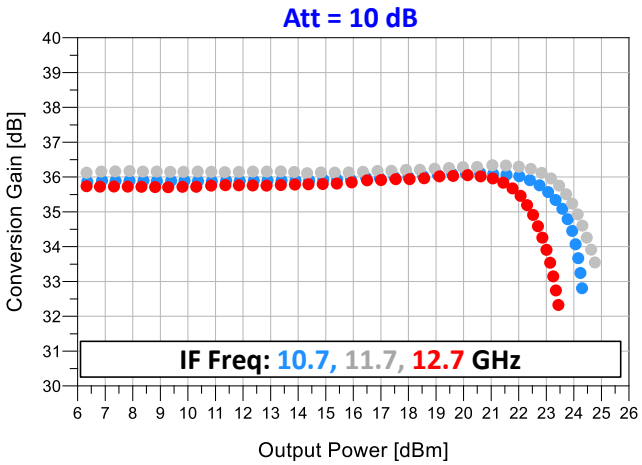


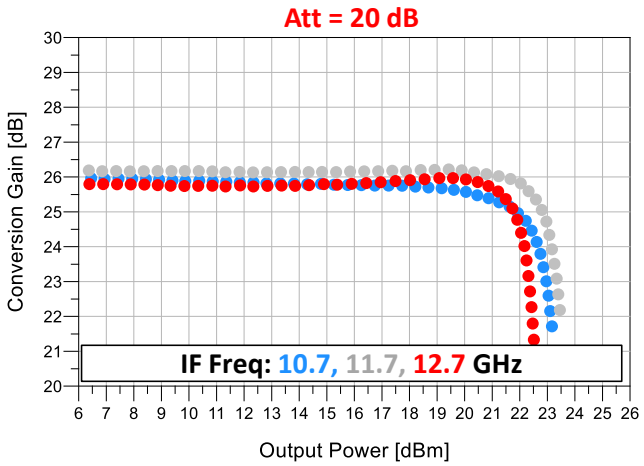
F_LO	F_RF worst	F_IF worst	Spurious Components				
			LO_ind	RF_ind	freq	f_distance	Att
1.3	14.50	13.20	-3	1	10.60	2.60	14.0
1.3	14.50	13.20	-2	1	11.90	1.30	17.0
1.3	13.00	11.70	9	0	11.70	0.00	60.0
1.8	13.00	11.20	6	0	10.80	0.40	32.0
1.8	14.50	12.70	0	1	14.50	1.80	27.0
1.8	14.50	12.70	7	0	12.60	0.10	32.0
2.3	13.75	11.45	5	0	11.50	0.05	32.0
2.3	13.50	11.20	-7	2	10.90	0.30	65.0
2.3	13.50	11.20	4	0	9.20	2.00	30.0
2.8	14.00	11.20	4	0	11.20	0.00	23.0
2.8	14.00	11.20	9	-1	11.20	0.00	27.0
2.8	14.00	11.20	-6	2	11.20	0.00	60.0
3.3	13.25	9.95	3	0	9.90	0.05	37.0
3.3	13.25	9.95	7	-1	9.85	0.10	25.0
3.3	13.25	9.95	-5	2	10.00	0.05	50.0
GHz	GHz	GHz			GHz	GHz	dBc

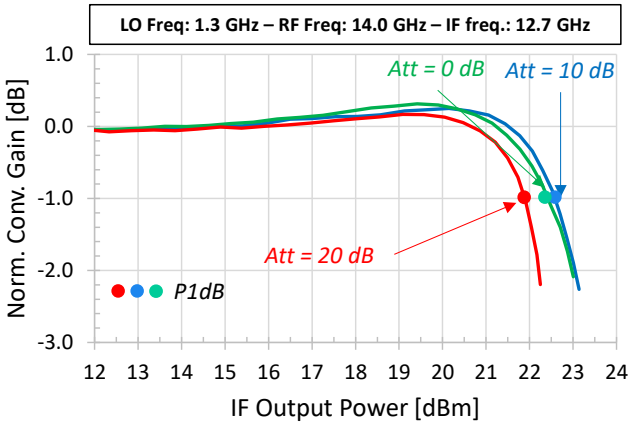
Main Performance – Gain Compression

VC = -2.2 V







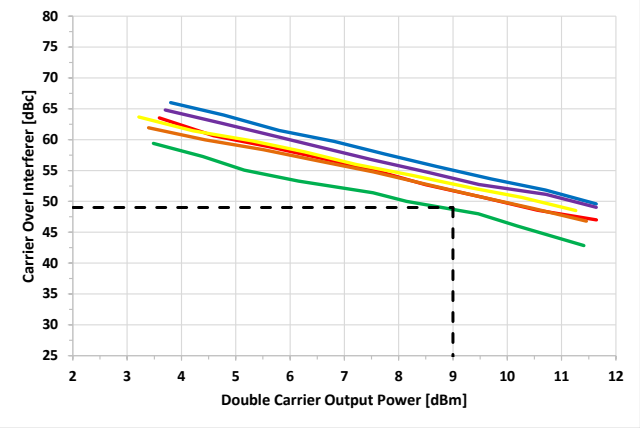


Main Performance – Intermodulation

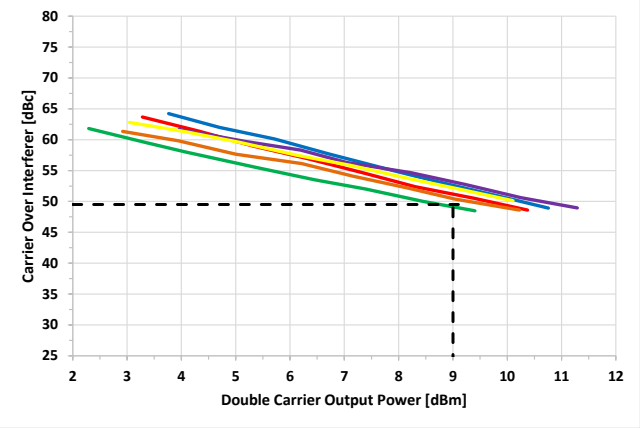
VC = -2.2 V; Δfreq = 10 MHz

IF Freq. 10.45GHz @LO Freq. 2.8 GHz
IF Freq. 10.95GHz @LO Freq. 2.3 GHz
IF Freq. 11.20GHz @LO Freq. 2.8 GHz
IF Freq. 11.45GHz @LO Freq. 1.8 GHz
IF Freq. 11.70GHz @LO Freq. 2.3 GHz
IF Freq. 12.20GHz @LO Freq. 1.8 GHz

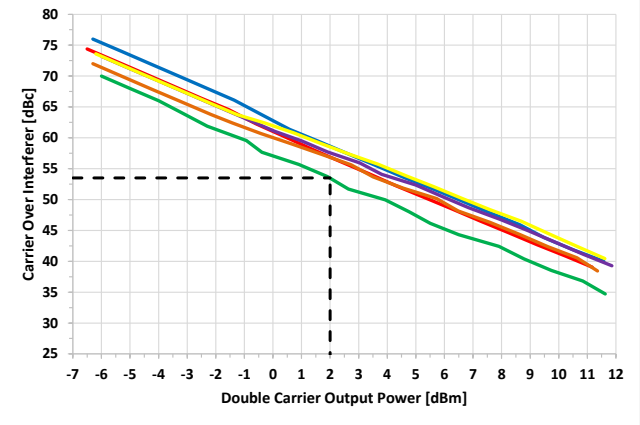
C/I3 Vs. Output Power @ Att. = 0 dB



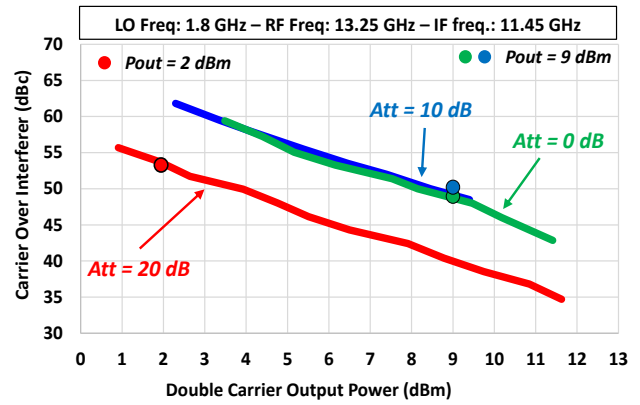
C/I3 Vs. Output Power @ Att. = 10 dB



C/I3 Vs. Output Power @ Att. = 20 dB



C/I3 Vs. Output Power @ IF = 17.25 GHz



TOI Vs. IF_freq @ Att. = 0, 10, 20 dB

TOI [dBm]			
IF freq. [GHz] \ ATT. [dB]	0	10	20
10.45	35	35	31
10.95	37	35	31
11.20	36	36	31
11.45	33	33	29
11.70	35	35	32
12.20	35	34	30

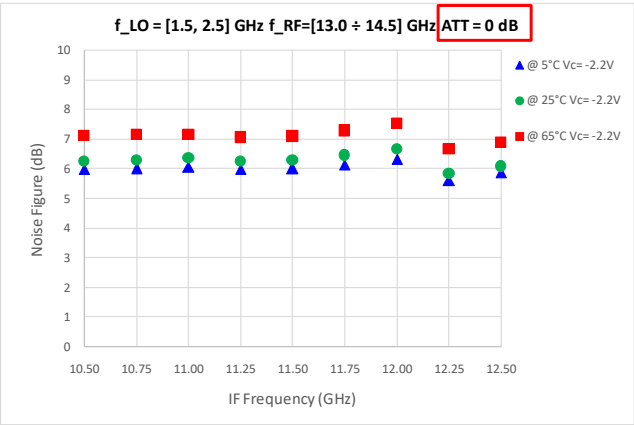
C/I3 Vs. IF_freq @ Att. = 0, 10, 20 dB

C/I3 [dBc]			
IF freq. [GHz] \ ATT. [dB]	0 @Pout 9dBm	10 @Pout 9dBm	20 @Pout 2dBm
10.45	51.5	51.5	57.0
10.95	55.0	53.0	58.0
11.20	54.0	53.0	57.0
11.45	49.5	49.5	53.0
11.70	52.5	52.0	58.0
12.20	52.0	50.5	57.0

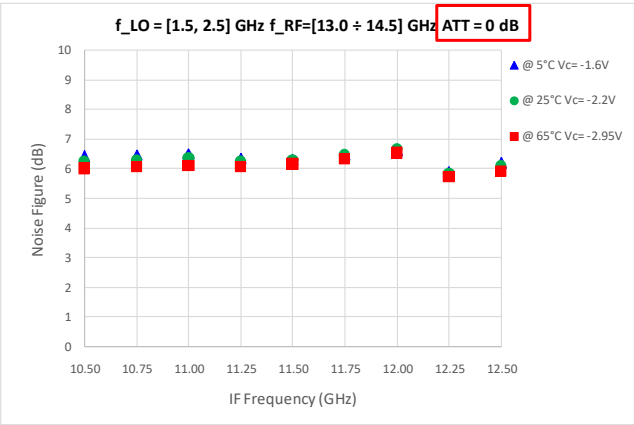
Main Performance – Noise Figure

Noise Figure with and without temperature compensation. 7 dB is the maximum attenuation enabled on RF input section.

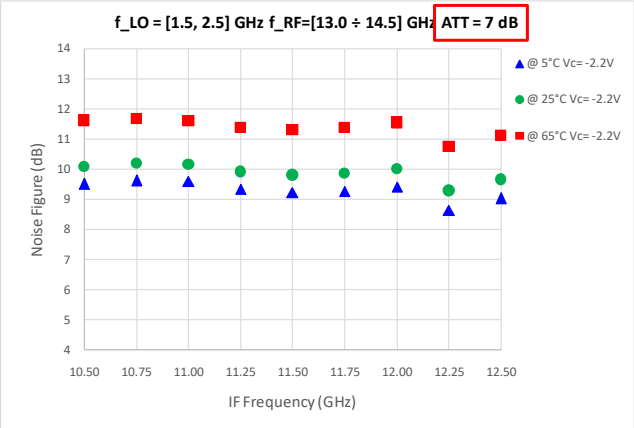
Noise Figure Vs. IF_freq @ 5, 25, 65 °C; **No compensation**
Att. = 0 dB



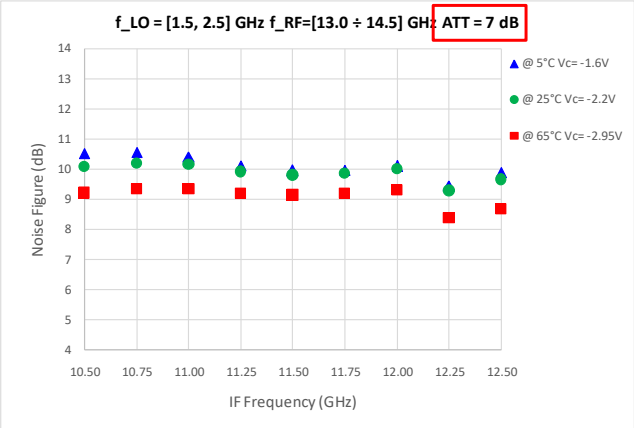
Noise Figure Vs. IF_freq @ 5, 25, 65 °C; **Compensation**
Att. = 0 dB



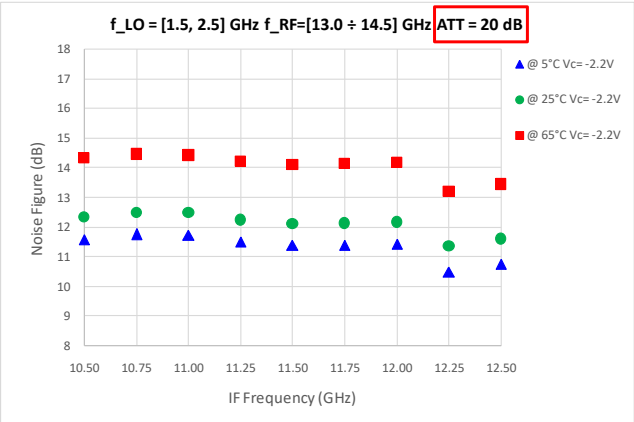
Noise Figure Vs. IF_freq @ 5, 25, 65 °C; **No compensation**
Att. = 7 dB



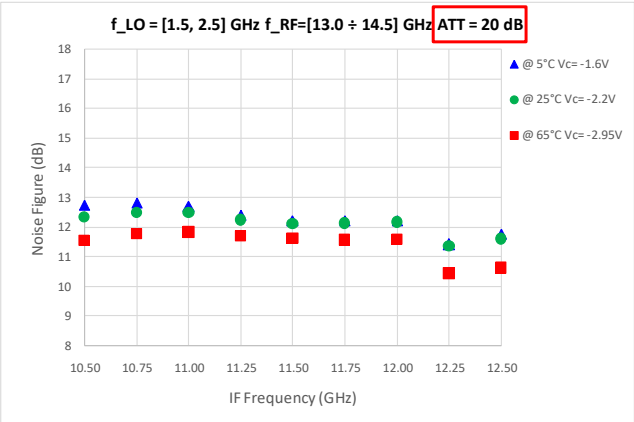
Noise Figure Vs. IF_freq @ 5, 25, 65 °C; **Compensation**
Att. = 7 dB



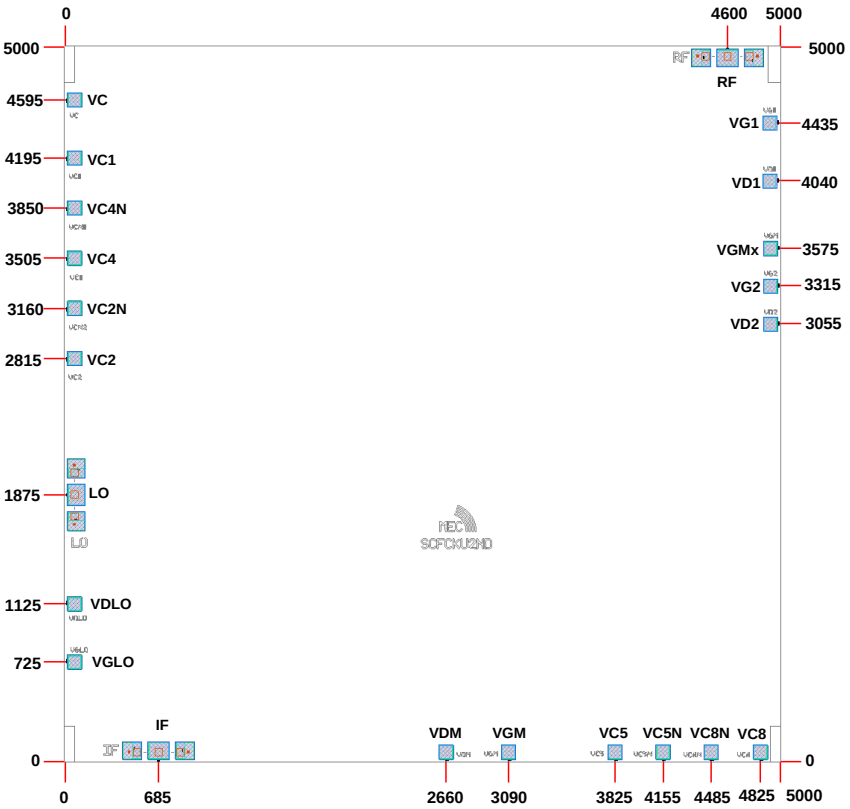
Noise Figure Vs. IF_freq @ 5, 25, 65 °C; **No compensation**
Att. = 20 dB



Noise Figure Vs. IF_freq @ 5, 25, 65 °C; **Compensation**
Att. = 20 dB



Mechanical information

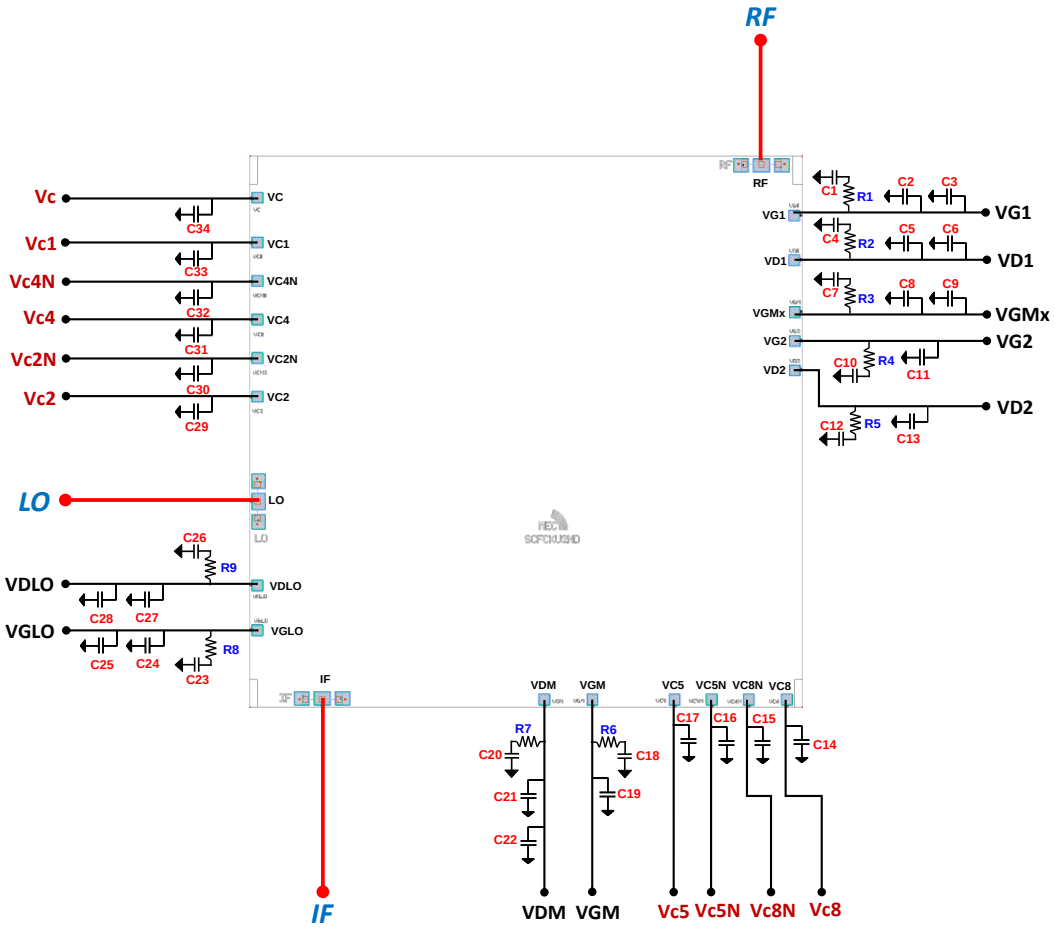


- Units: micrometres (µm)
- Chip dimensions: 5000 µm x 5000 µm ± 35 µm
- Chip Thickness is 70 µm ± 5 µm
- Chip edge to bond pad dimensions are shown to center of pad
- Ground is backside of die

Bond Pad Description

Bond Pad #	Pad Size (µm)	Description
RF	150 x 120	Input RF Port
VC	100 x 100	Control Voltage for temperature compensation. Levels' range at p. 2
VC1, VC4N, VC4, VC2N, VC2	100 x 100	Control Voltages for first section of step attenuation. Levels configuration at p. 2.
LO	150 x 120	LO input Port
VDLO, VGLO	100 x 100	Drain and Gate Bias for LO Buffer. Typ. values and current at p. 2.
IF	150 x 120	Output IF Port
VDM, VGM	100 x 100	Drain and gate Bias for Amplification stage at IF output. Typ. values and current at p. 2.
VGB, VDB	100 x 100	Gate and Drain Bias for RF Buffer. Typ. values and current at p. 2.
VC5, VC5N, VC8n, VC8	100 x 100	Control Voltages for second section of attenuation. Levels configuration at p. 2.
VD2, VG2	100 x 100	Drain and gate Bias for Amplification stage at IF output. Typ. values and current at p. 2.
VGMx	100 x 100	Gate control voltage for the Mixer. Typ. value at p. 2.
VD1, VG1	100 x 100	Drain and Gate Bias for Buffer amplifier at RF input. Typ. values and current at p. 2.

Assembly Plan



Ref.	Component	Value	Description
C1, C4, C14, C15, C16, C17, C20, C29, C30, C31, C32, C33, C34	SMT Capacitor	100 pF	Low Frequency Bypass Capacitor
C2, C5, C7, C23, C26	SMT Capacitor	1 nF	Low Frequency Bypass Capacitor
C10, C12, C18, C21	SMT Capacitor	10 nF	Low Frequency Bypass Capacitor
C8, C24, C27	SMT Capacitor	100 nF	Low Frequency Bypass Capacitor
C3, C6, C9, C11, C13, C19, C22, C25, C28	SMT Capacitor	1 µF	Low Frequency Bypass Capacitor
R1….R9	SMT Resistor	5 Ω	Low power Resistor

Bias-up Procedure

1. Set all VG to -1.5 V.
2. Set all VD to +4 V.
3. Set VC to typical value indicated in table at p. 2 (Typical -1.8 V)
4. Set all Vc for 0 dB Attenuation as per Gain Control table at p. 2.
5. Adjust VGs to get Id currents as per values in table at p. 2. (Vg = -0.65 V Typical).
6. Apply RF signals.

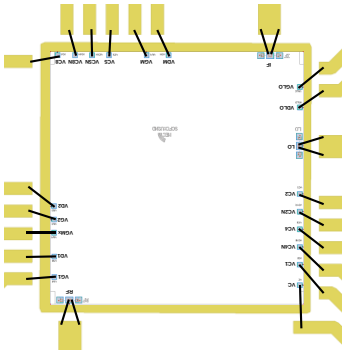
Bias-down Procedure

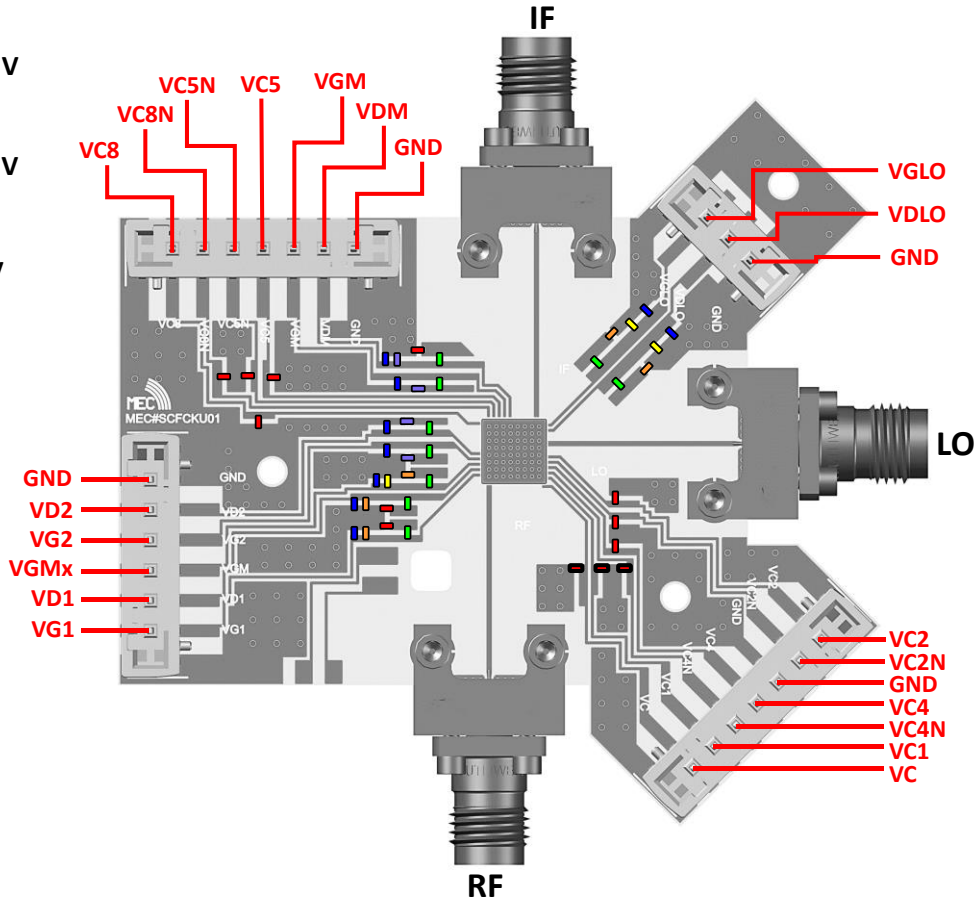
1. Turn off RF signals.
2. Reduce VG to -1.5 V (Id0 ≈ 0 mA).
3. Set all voltages to 0 V.

Evaluation Board and Bonding Diagram

CAP 0402, 100 nF, 10 V
CAP 0402, 1 uF, 10 V
CAP 0402, 100 pF, 10 V
CAP 0402, 1 nF, 10 V
CAP 0402, 10 nF, 10 V
RES 0402, 5 Ohm

Bonding Diagram





0.008" thick Rogers Corp. RO4003C (ε_r = 3.35). Metal layers 0.5 oz. copper cladding. Microstrip to Coplanar transition optimized to access the package. Microstrip to coplanar transition for connector interface optimized for the Southwest Microwave end launch 1492-04A-5.

Assembly Guideline

The backside of the MMIC is RF ground. Die attach should be accomplished with electrically and thermally conductive epoxy only. Eutectic attach is not recommended. Follow manufacture instructions for epoxy curing.

Standard assembly procedures should be followed for high frequency devices. The top surface of the semiconductor should be made planar to the adjacent RF transmission lines. Vacuum pencils and/or vacuum collets are the preferred method of pick up. Do not make contact directly with the die surface as this will damage the monolithic circuitry. Air bridges must be avoided during placement. Handle with care.

RF connections should be made as short as possible to reduce the inductive effect of the bond wire. Use of a 25 µm thermosonic wedge bonding is highly recommended as the loop height will be minimized. Force, time, and ultrasonic are critical parameters.

RoHS Compliance

The product is compliant with the 2011/65/EU RoHS directive 2015/863/EU and REACH N° 1907/2006.

Contact Information

For additional technical Information and Requirements: **contact.mec@mec-mmic.com**

Notice

The furbished information is believed to be reliable. However, performances and specifications contained herein are based on preliminary characterizations and then susceptible to possible variations. On the basis of customer requirements, the product can be tested and characterized in specific operating conditions and, if needed, tuned to meet custom specifications.