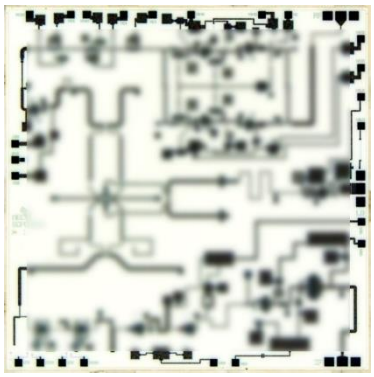
MECKaSCFC

Ka-to-Ka Single Chip Frequency Converter



Product Description

MECKaSCFC is a Ka-to-Ka band full frequency high-linearity downconverter. It is based on a 0.15 µm GaAs pHEMT space evaluated process.

The MECKaSCFC integrates in a single MMIC up to 8 different operating blocks to provide, in addition to the frequency conversion, programmable Gain control, compensation of gain variation over temperature, RF, IF and LO signals amplification.

In the IF frequency band [17.2 – 20.2] GHz, synthesized by LO frequencies in the range [4.65 – 6.10] GHz and RF frequency in the band [27.5 – 30.0] GHz, the MECKaSCFC offers a conversion gain of about 43 dB, an output power of 23 dBm at 1 dB of gain compression and an output TOI of 33 dBm. A 20 dB programmable gain attenuation, with 1 dB steps, and a continuous 7 dB fine tuning, to fully compensate the gain variation over temperature, are also integrated in the chip.

It is available in a 5x5 mm^2 bare die.

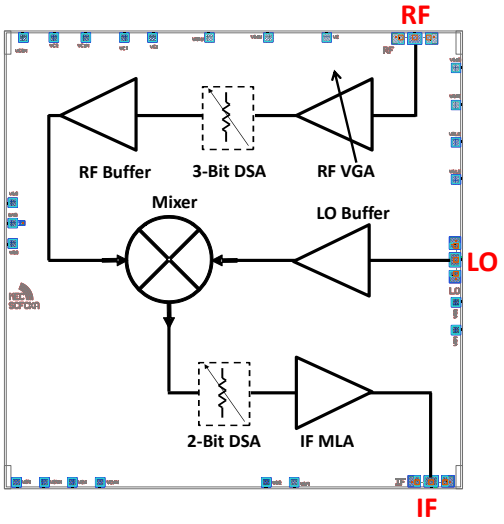
Applications

Telecom Satellite Applications

Main Features

- 0.15µm GaAs pHEMT space evaluated process
- Full performance in the frequency bands:
  - RF: 27.5 - 30 GHz
  - LO: 4.5 – 6.2 GHz
  - IF: 17.2 – 20.2 GHz
- +23 to +43 dB minimum Conversion Gain
- 20 dB Gain variation 1 dB step
- 8 dB of continuous Gain variation for temperature compensation
- Linear operating Output Power from -4 to 7 dBm
- C/I3 of 50 dBc at 7 dBm of output power
- Power consumption of 1.16 W
- Fixed Bias: VDD = 4V, Idq = 290 mA
- 9 control signals (-1.5 V; 0 V) to implement the 20 dB Gain variation 1 dB step
- Control voltage VC in the range [-4 – 0] V to perform the compensation over temperature
- Fully matched to 50 Ω, with integrated RF to DC decoupling
- Chip Size: 5.0 x 5.0 x 0.07 mm^3

Functional Block Diagram



Nominal Operating Conditions

Parameter	Min	Typ.	Max	Units
Temperature Range	-20	+30	+70	°C
VG1U, VG1D		-0.65		V
VD1U, VD1D		4		V
ID1Uq, ID1Dq		42		mA
VGLO		-0.65		V
VDLO		4		V
IDLOq		31		mA
VG2		-0.65		V
VD2		4		V
ID2q		41		mA
VGM		-0.65		V
VDM		4		V
IDMq		110		mA
VGB		-0.65		V
VDB		4		V
IDBq		21		mA
VC	-4	-1.8	0	V
VC1	-1.5	*	0	V
VC2	-1.5	*	0	V
VC2N	-1.5	*	0	V
VC4	-1.5	*	0	V
VC4N	-1.5	*	0	V
VC5	-1.5	*	0	V
VC5N	-1.5	*	0	V
VC8	-1.5	*	0	V
VC8N	-1.5	*	0	V
PLO	0	1	3	dBm
PDC		1.16		W

- When operates under these recommended conditions, the device is compliant with ESA space-derating rules.
- Electrical specifications are measured at specified test conditions.
- The continuous Gain variation features can be achieved by applying a continuous variation to VC.
- The 20 dB Gain variation/attenuation, 1-dB step, can be implemented according to the following Control Table

Gain Control Table

Att	VC1	VC2	VC2N	VC4	VC4N	VC5	VC5N	VC8	VC8N
dB	*V*	*V*	*V*	*V*	*V*	*V*	*V*	*V*	*V*
0	0	0	-1.5	0	-1.5	0	-1.5	0	-1.5
1	-1.5	0	-1.5	0	-1.5	0	-1.5	0	-1.5
2	0	-1.5	0	0	-1.5	0	-1.5	0	-1.5
3	-1.5	-1.5	0	0	-1.5	0	-1.5	0	-1.5
4	0	0	-1.5	-1.5	0	0	-1.5	0	-1.5
5	-1.5	0	-1.5	-1.5	0	0	-1.5	0	-1.5
6	0	-1.5	0	-1.5	0	0	-1.5	0	-1.5
7	-1.5	-1.5	0	-1.5	0	0	-1.5	0	-1.5
8	-1.5	-1.5	0	0	-1.5	-1.5	0	0	-1.5
9	0	0	-1.5	-1.5	0	-1.5	0	0	-1.5
10	-1.5	0	-1.5	-1.5	0	-1.5	0	0	-1.5
11	0	-1.5	0	-1.5	0	-1.5	0	0	-1.5
12	-1.5	-1.5	0	-1.5	0	-1.5	0	0	-1.5
13	0	0	-1.5	0	-1.5	-1.5	0	-1.5	0
14	-1.5	0	-1.5	0	-1.5	-1.5	0	-1.5	0
15	0	-1.5	0	0	-1.5	-1.5	0	-1.5	0
16	-1.5	-1.5	0	0	-1.5	-1.5	0	-1.5	0
17	0	0	-1.5	-1.5	0	-1.5	0	-1.5	0
18	-1.5	0	-1.5	-1.5	0	-1.5	0	-1.5	0
19	0	-1.5	0	-1.5	0	-1.5	0	-1.5	0
20	-1.5	-1.5	0	-1.5	0	-1.5	0	-1.5	0

Absolute Maximum Rating

Parameter	Rating
VD	8 V
VG / VC	-2.5 to 0 V
Channel temperature, T_J	175 °C
PDC (T = 85 °C; VD = 4V)	1.5 W
RF Input Power	-8 dBm
LO Input Power	8 dBm
Mounting Temperature (<30 sec)	260 °C
Storage Temperature	-55 to +150 °C

These parameters are carried out from stress test analysis and foundry data.

Thermal and Reliability Information

Conditions	Parameter	Value
Nominal Bias Tbase = +70 °C Worst Case (wc): - Pdiss = 1.16 W (PLO not applied)	Equivalent Thermal Resistance	43 °C/W
	Channel Temperature	120 °C (wc)
		110 °C (nc)
Nominal Condition (nc): - Pdiss = 0.93 W (PLO = 3 dBm)	**Mean Time Failure**	**> 2E+7 hrs**

Electrical Characteristics

Test conditions unless otherwise noted: Tbase = 30°C; Bias, typical values in previous table.

Parameter	Min.	Typ	Max	Units
Input Frequency Range (RF)	27.5		30.0	GHz
Output Frequency Range (IF)	17.2		20.2	GHz
LO Frequency Range (LO)	4.5		6.2	GHz
Operating RF Input levels	-55		-25	dBm
Overdrive survivability at RF port			-8	dBm
LO Input Power Range	2	3	4	dBm
Conversion Gain	24		44	dB
Gain Step		1		dB
Gain Stability				
Over any 15°C		0.1		dBpp
Over acceptance temp. range		1		dBpp
Over life (Excluding temperature effects)		0.7		dBpp
Gain Flatness				
Over any 500 MHz		0.5		dBpp
Over operational range		1.0		dBpp
Gain Slope		0.01		dB/MHz
Noise Figure				
Max Gain		7.5		dB
Min Gain		18		dB
Output P1dB				
Max Gain		+23		dBm
Min Gain		+19		dBm
Output IP3 level				
Max Gain	+32.5		+34.5	dBc
Min Gain	+28.5		+31.0	dBc
Amplitude Linearity - C/I3				
Max Gain (@ Pout = 7 dBm)	51		56	dBc
Min Gain (@ Pout = -3 dBm)	64		67	dBc
Single Carrier Spurious				
In-Band Spurious		-80 (1)		dBc
Out of Band Spurious		-16 (2)		dBc
LO harmonics attenuation		27		dBc
Output Return Loss	10			dB
Input Return Loss	10			dB
Power Consumption			1.16	W

(1) For specific frequency schemes
(2) 2.7 GHz below the IF band

Test Conditions

Test conditions unless otherwise noted: Tbase = 30°C, (VD1U, VD1D, VDLO, VD2, VDM, VDB) = 4 V, ID1Uq = ID1Dq = 84 mA, IDLOq = 31 mA (IDLO = 34 mA @ PLOin = 3 dBm), ID2q = 41 mA, IDMq = 110 mA, IDBq = 21 mA, VC (nominal) = -1.8 V, P_LO = 3 dBm. Control Voltages for Gain Variation applied as per "Gain Control Table". P_RF as per table below.

Gain & Power variation scheme

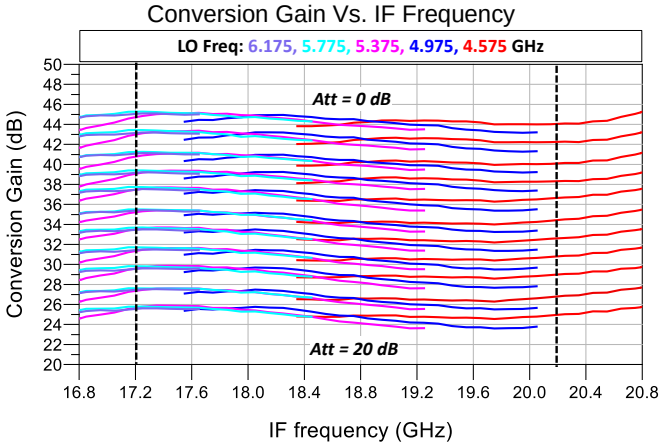
Reference Gain	*44*	*43*	*42*	*41*	*40*	*39*	*38*	*37*	*36*	*35*	*34*	*33*	*32*	*31*	*30*	*29*	*28*	*27*	*26*	*25*	*24*	*dB*
Input Level	-37	-36	-35	-34	-33	-32	-31	-30	-29	-28	-27	-26	-25	-25	-25	-25	-25	-25	-25	-25	-25	dBm
DSA Att.	0	-1	-2	-3	-4	-5	-6	-7	-8	-9	-10	-11	-12	-13	-14	-15	-16	-17	-18	-19	-20	dB
Nominal Pout	7	7	7	7	7	7	7	7	7	7	7	7	7	6	5	4	3	2	1	0	-1	dBm

Adopted Conversion Scheme

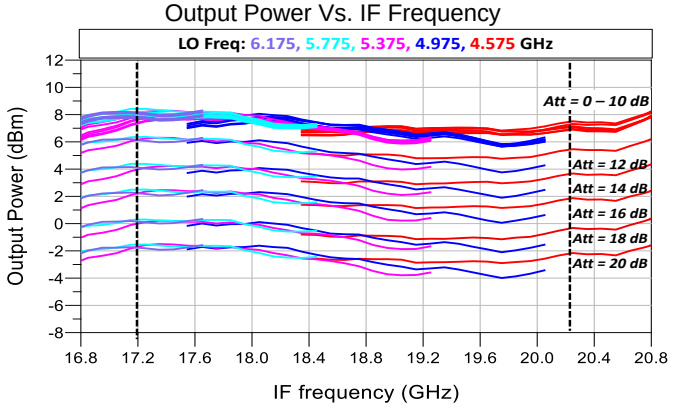
LO freq	4.575	4.975	5.375	5.775	6.175	GHz
Syn. #	1	2	3	4	5	
RF freq	IF freq.					
27.5	18.35	17.55	16.75	15.95	15.15	
28.0	18.85	18.05	17.25	16.45	15.65	
28.5	19.35	18.55	17.75	16.95	16.15	
29.0	19.85	19.05	18.25	17.45	16.65	
29.5	20.35	19.55	18.75	17.95	17.15	
30.0	20.85	20.05	19.25	18.45	17.65	
GHz	GHz	GHz	GHz	GHz	GHz	

Main Performance – Conversion Gain and Output Power

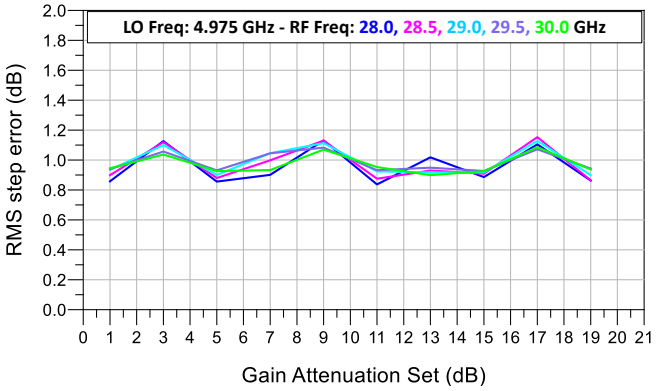
Conversion Gain Vs. IF Frequency



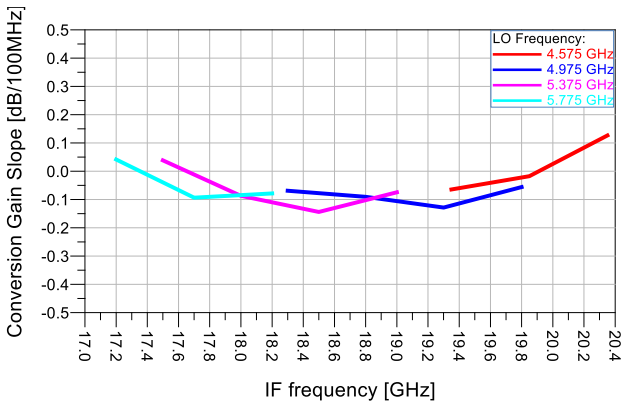
Output Power Vs. IF Frequency



Gain varition step error

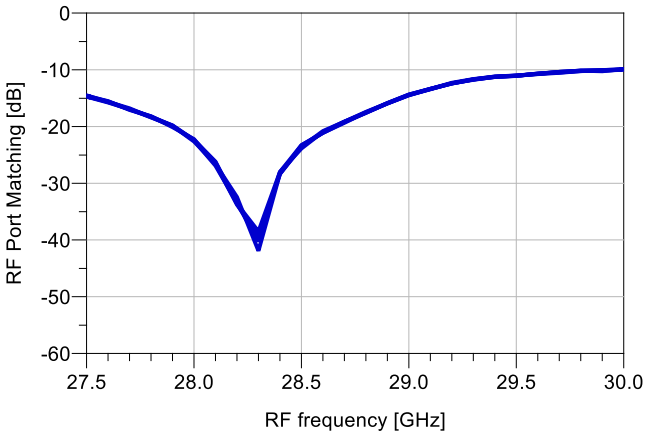


Output Power Vs. IF Frequency

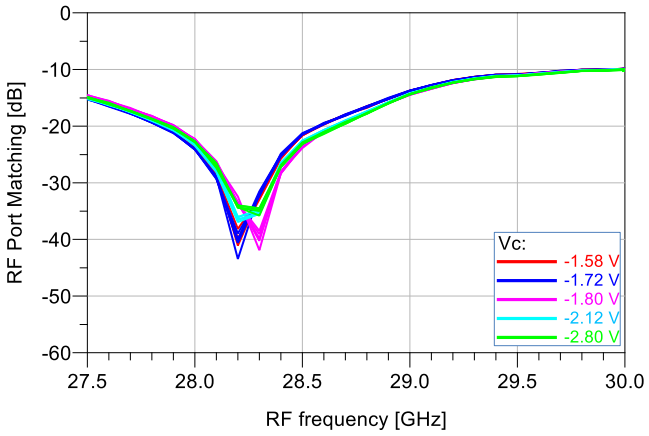


Main Performance – Port Matching

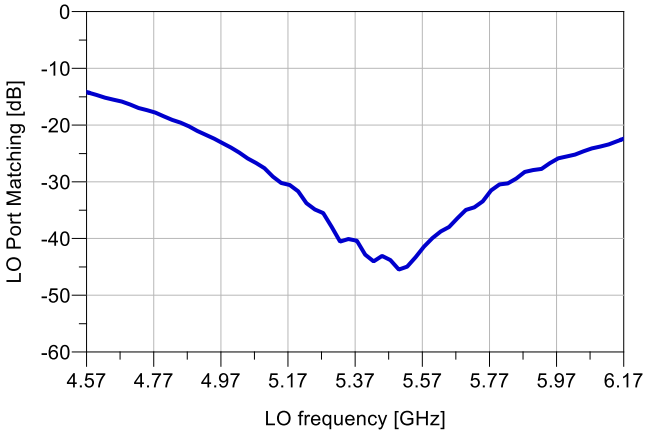
Return Loss @ RF Input port



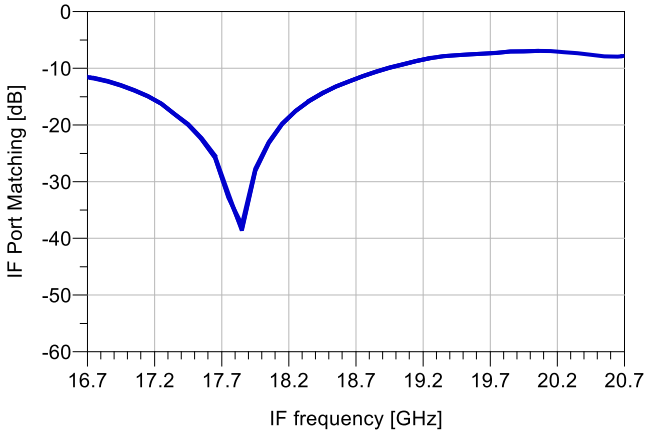
Return Loss @ RF input port Vs. Vc



Return Loss @ LO port



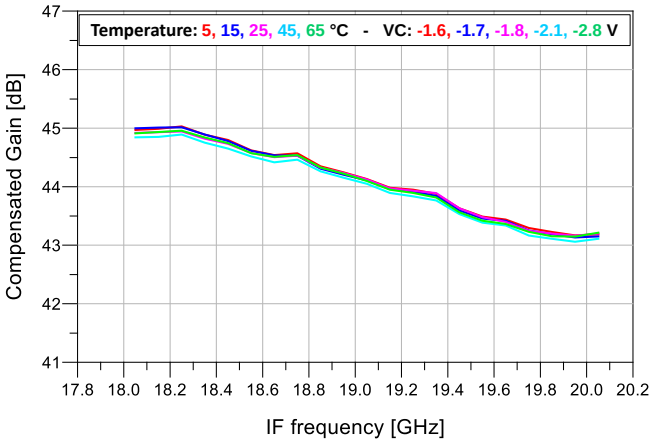
Return Loss @ IF output port



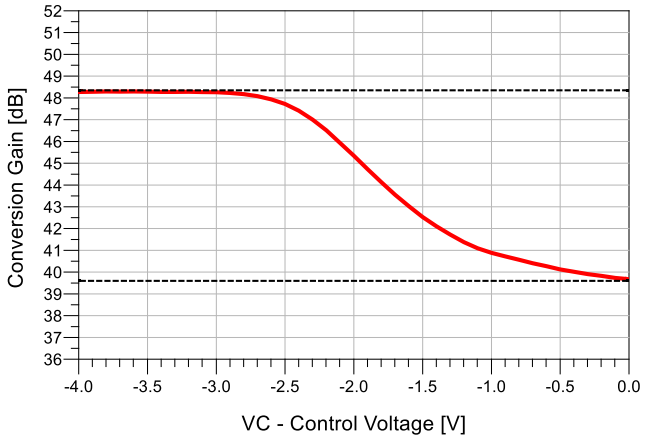
Main Performance – Conversion Gain Vs. Temperature

FLO = 4.975 GHz, FRF = [28 – 30] GHz, Attenuation = 0 dB

Conversion Gain Vs. IF Frequency

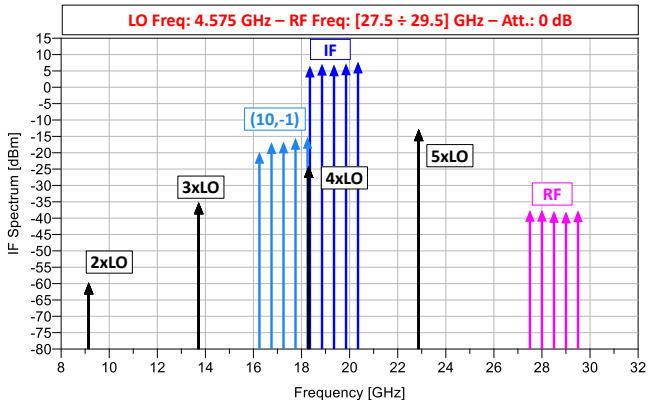


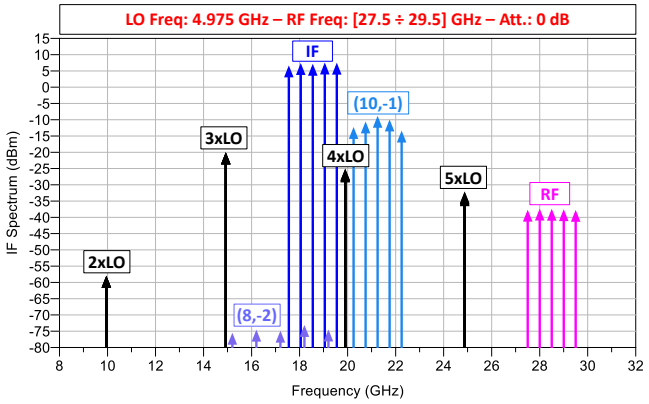
Output Power Vs. IF Frequency

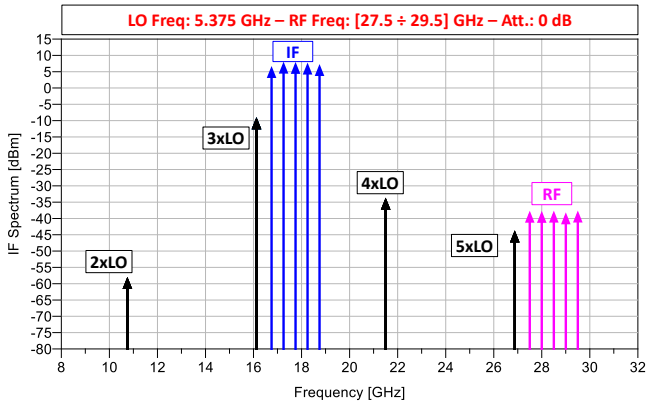


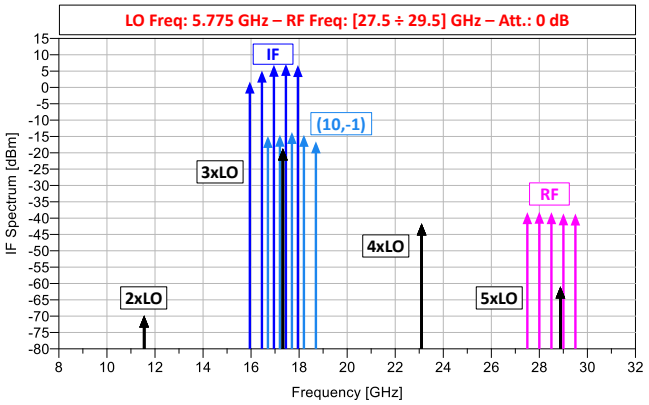
Main Performance – Output Spectrum

FRF = [27.5 – 29.5] GHz, Attenuation = 0 dB, VC = -1.8 V





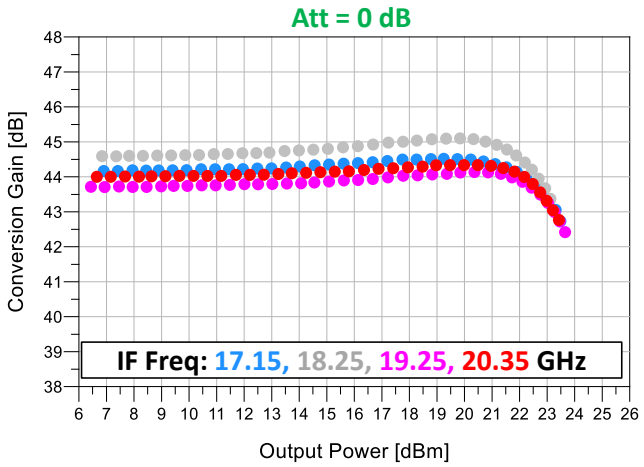


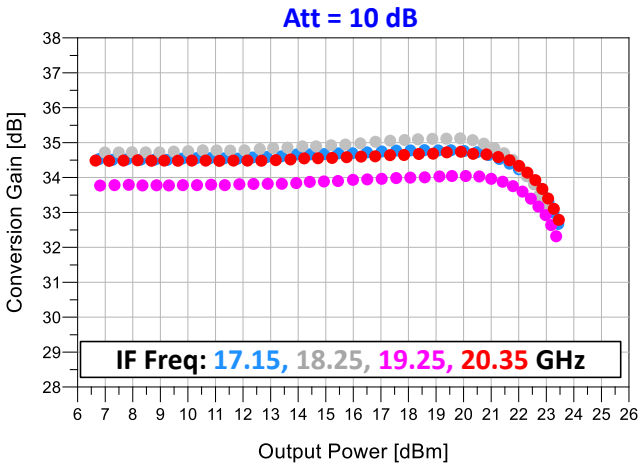


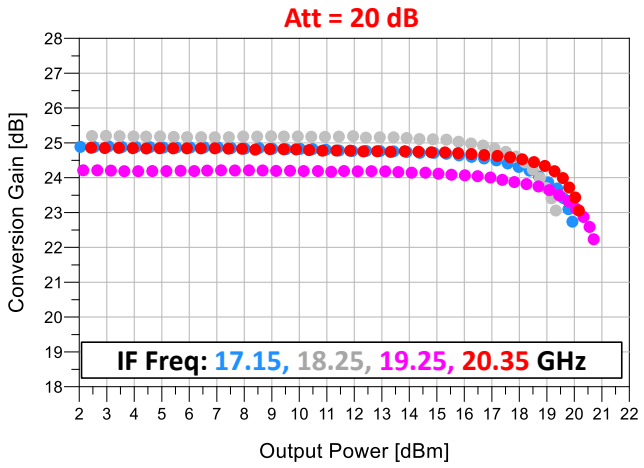
F_LO	F_RF worst	F_IF worst	Spurious Components				
			LO_ind	RF_ind	freq	f_distance	Att
4.575	27.5	18.35	10	-1	18.250	100	22.7
4.575	27.5	18.35	4	0	18.300	50	31.9
4.575	27.5	18.35	5	0	22.875	4525	21.1
4.975	30.0	20.05	10	-1	19.750	300	21.8
4.975	30.0	20.05	4	0	19.900	150	34.2
4.975	30.0	20.05	-8	2	20.200	150	81.8
5.375	27.5	16.75	3	0	16.125	625	16.6
5.375	27.5	16.75	8	-1	15.500	1250	33.8
5.375	27.5	16.75	-7	2	17.375	625	68.9
5.775	29.0	17.45	8	-1	17.200	250	22.4
5.775	29.0	17.45	3	0	17.325	125	26.9
5.775	29.0	17.45	-12	3	17.700	250	70.4
6.175	30.0	17.65	3	0	18.525	875	21.0
6.175	30.0	17.65	8	-1	19.400	1750	24.6
6.175	30.0	17.65	-7	2	16.775	875	65.2
GHz	GHz	GHz			GHz	MHz	dBc

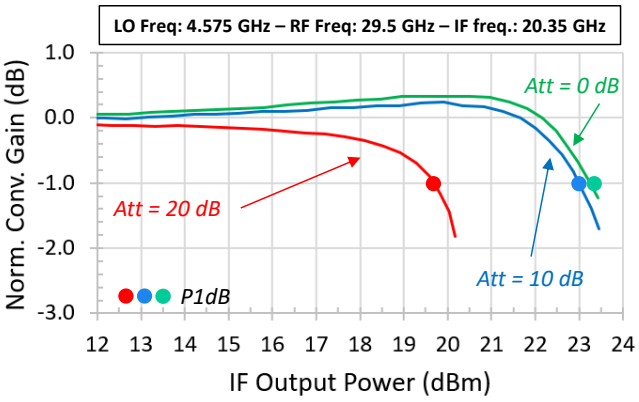
Main Performance – Gain Compression

VC = -1.8 V





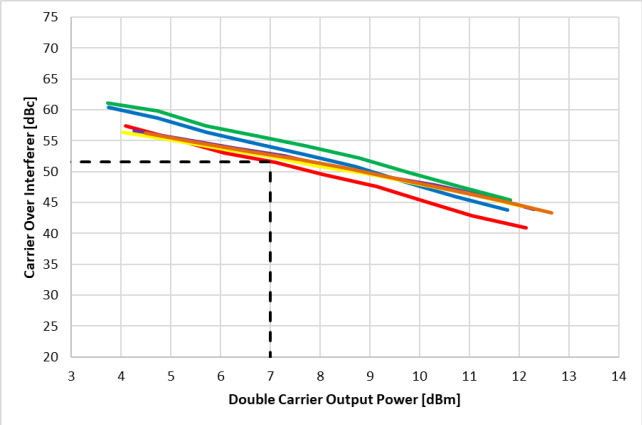




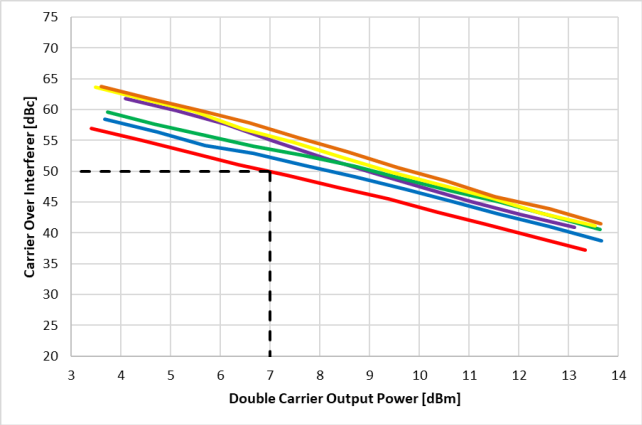
Main Performance – Intermodulation

VC = -1.8 V; Δfreq = 10 MHz

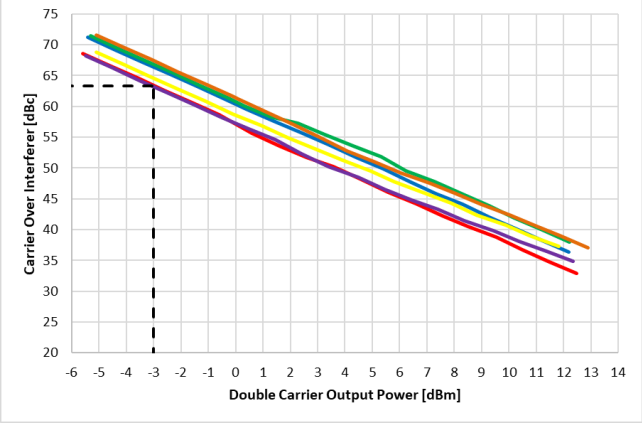
C/I3 Vs. Output Power @ Att. = 0 dB



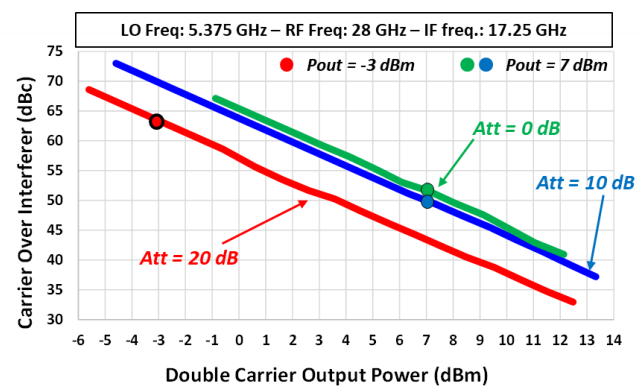
C/I3 Vs. Output Power @ Att. = 10 dB



C/I3 Vs. Output Power @ Att. = 20 dB



C/I3 Vs. Output Power @ IF = 17.25 GHz



TOI Vs. IF_freq @ Att. = 0, 10, 20 dB

TOI [dBm]			
IF freq. [GHz] \ ATT. [dB]	0	10	20
17.25	32.7	32.0	28.7
18.05	33.9	33.1	30.3
18.50	33.6	34.2	29.0
18.85	34.6	33.9	31.0
19.30	33.4	34.7	29.8
20.10	33.7	35.0	30.9

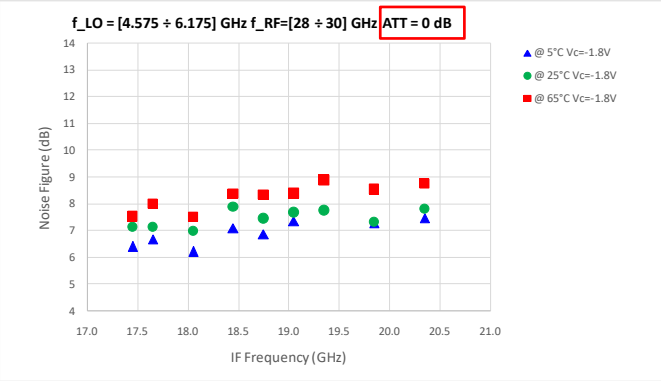
C/I3 Vs. IF_freq @ Att. = 0, 10, 20 dB

C/I3 [dBc]			
IF freq. [GHz] \ ATT. [dB]	0 @Pout 7dBm	10 @Pout 7dBm	20 @Pout -3dBm
17.25	51.6	49.4	64.6
18.05	54.5	52.9	67.2
18.50	52.6	54.9	64.2
18.85	55.8	54.0	67.4
19.30	52.5	54.7	64.8
20.10	53.3	57.9	67.6

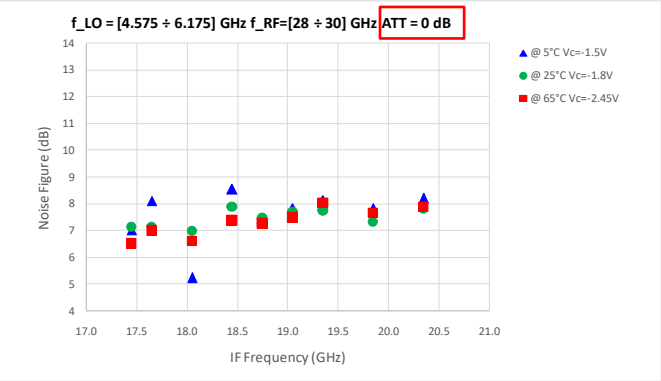
Main Performance – Noise Figure

Noise Figure with and without temperature compensation. 7 dB is the maximum attenuation enabled on RF input section.

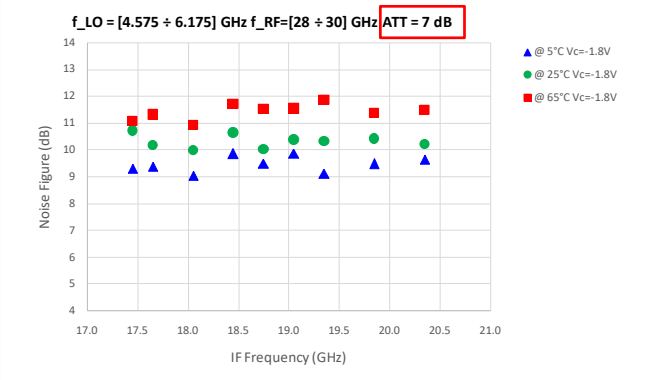
Noise Figure Vs. IF_freq @ 5, 25, 65 °C; **No compensation**
Att. = 0 dB



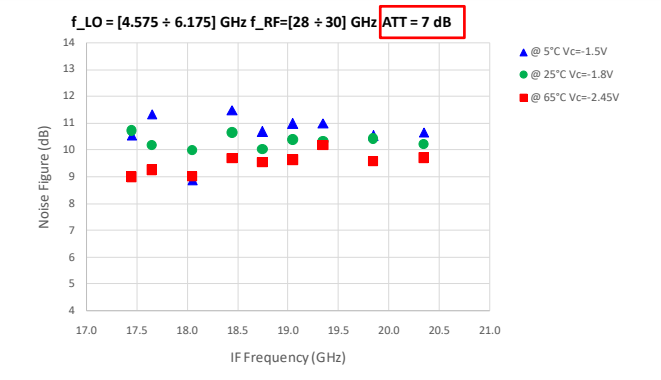
Noise Figure Vs. IF_freq @ 5, 25, 65 °C; **Compensation**
Att. = 0 dB



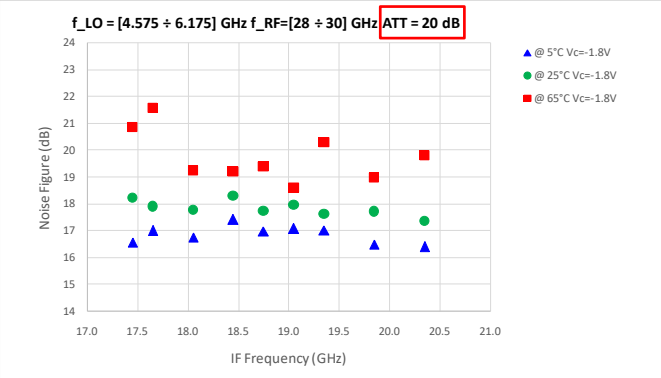
Noise Figure Vs. IF_freq @ 5, 25, 65 °C; **No compensation**
Att. = 7 dB



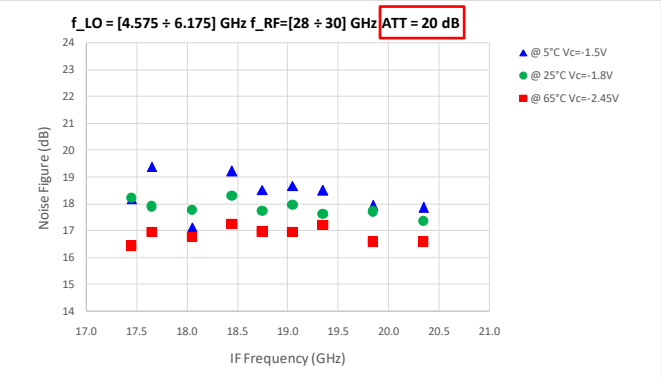
Noise Figure Vs. IF_freq @ 5, 25, 65 °C; **Compensation**
Att. = 7 dB



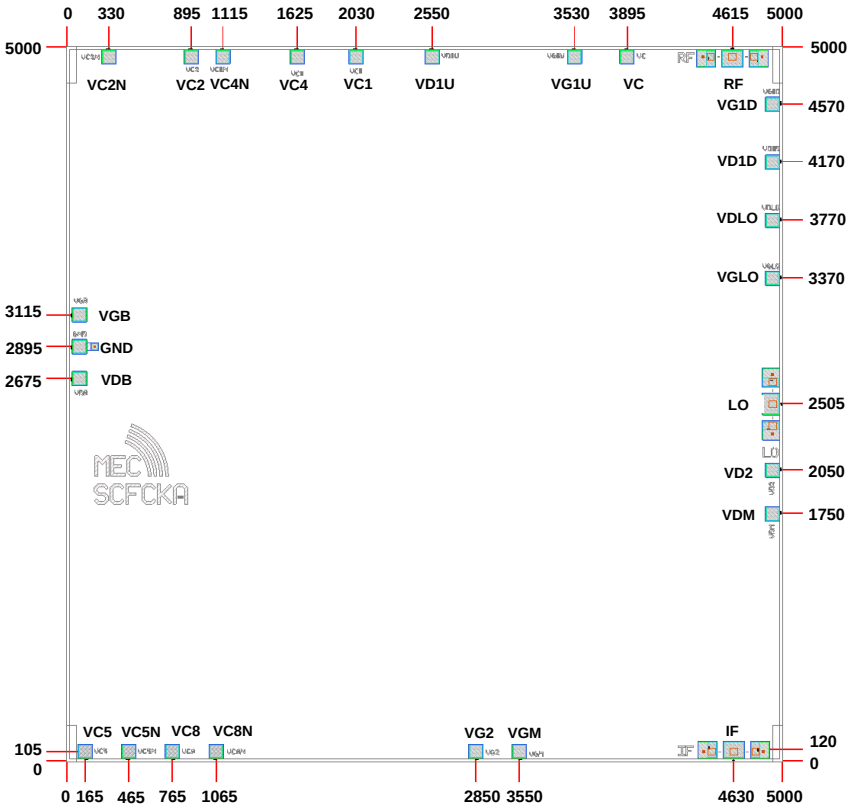
Noise Figure Vs. IF_freq @ 5, 25, 65 °C; **No compensation**
Att. = 20 dB



Noise Figure Vs. IF_freq @ 5, 25, 65 °C; **Compensation**
Att. = 20 dB



Mechanical information

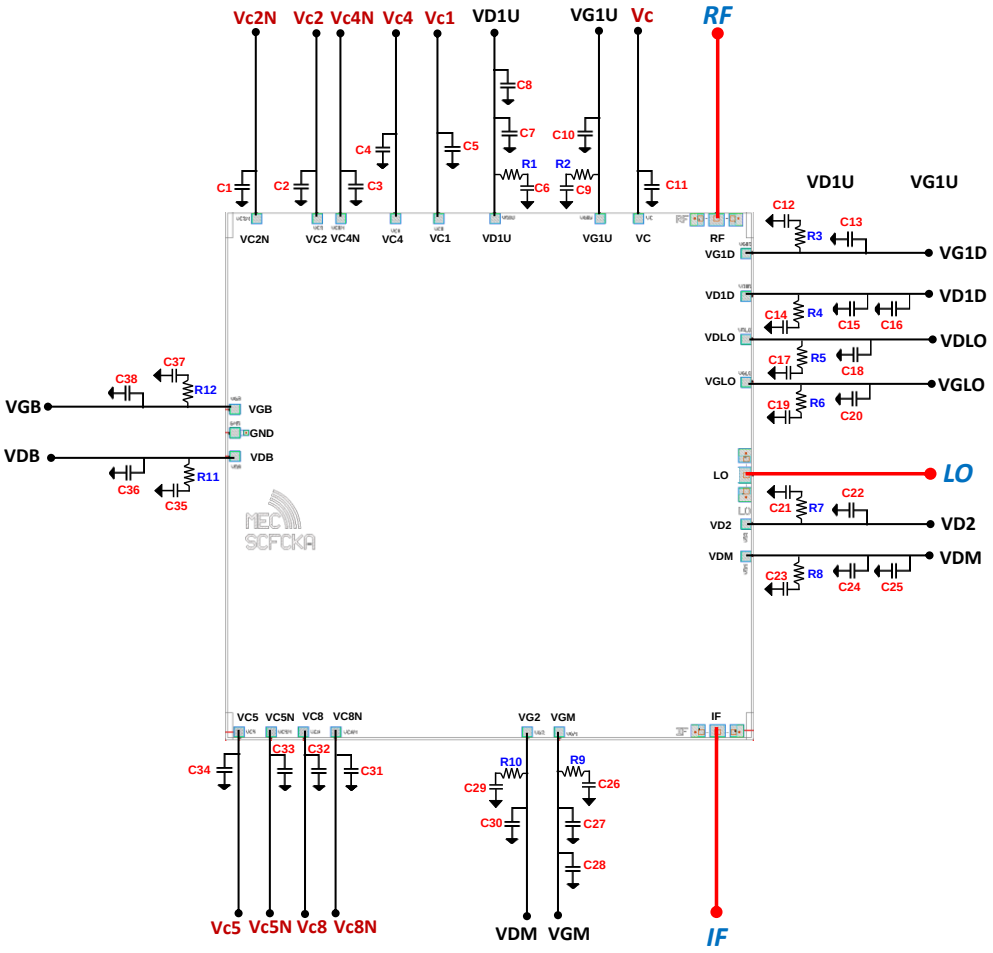


- Units: micrometres (µm)
- Chip dimensions: 5000 µm x 5000 µm ± 35 µm
- Chip Thickness is 70 µm ± 5 µm
- Chip edge to bond pad dimensions are shown to center of pad
- Ground is backside of die

Bond Pad Description

Bond Pad #	Pad Size (µm)	Description
RF	150 x 120	Input RF Port
VC	100 x 100	Control Voltage for temperature compensation. Levels' range at p. 2
VG1U, VD1U, VG1D, VD1D	100 x 100	Gate and Drain Bias for Buffer amplifier at RF input. Typ. values and current at p. 2.
VC1, VC4, VC4N, VC2, VC2N	100 x 100	Control Voltages for first section of step attenuation. Levels configuration at p. 2.
VGB, VDB	100 x 100	Gate and Drain Bias for RF Buffer. Typ. values and current at p. 2.
VC5, VC5N, VC8, VC8N	100 x 100	Control Voltages for second section of attenuation. Levels configuration at p. 2.
VG2, VD2, VGM, VDM	100 x 100	Gate and Drain Bias for Amplification stages at IF output. Typ. values and currents at p. 2.
IF	150 x 120	Output IF Port
LO	150 x 120	LO input Port
VGLO, VDLO	100 x 100	Gate and Drain Bias for LO Buffer. Typ. values and current at p. 2.

Assembly Plan



Ref.	Component	Value	Description
C1, C2, C3, C4, C5, C6, C9, C11, C12, C14, C21, C23, C26, C29, C31.C32, C33, C34, C35, C37	SMT Capacitor	100 pF	Low Frequency Bypass Capacitor
C7, C10, C13, C15, C24, C27	SMT Capacitor	1 nF	Low Frequency Bypass Capacitor
C8, C16, C18, C20, C22, C25, C28, C30, C36, C38	SMT Capacitor	1 µF	Low Frequency Bypass Capacitor
R1….R12	SMT Resistor	5 Ω	Low power Resistor

Bias-up Procedure

1. Set all VG to -1.5 V.
2. Set all VD to +4 V.
3. Set VC to typical value indicated in table at p. 2 (Typical -1.8 V)
4. Set all Vc for 0 dB Attenuation as per Gain Control table at p. 2.
5. Adjust VGs to get Id currents as per values in table at p. 2. (Vg = -0.65 V Typical).
6. Apply RF signals.

Bias-down Procedure

1. Turn off RF signals.
2. Reduce VG to -1.5 V (Id0 ≈ 0 mA).
3. Set all voltages to 0 V.

Assembly Guideline

The backside of the MMIC is RF ground. Die attach should be accomplished with electrically and thermally conductive epoxy only. Eutectic attach is not recommended. Follow manufacture instructions for epoxy curing.

Standard assembly procedures should be followed for high frequency devices. The top surface of the semiconductor should be made planar to the adjacent RF transmission lines. Vacuum pencils and/or vacuum collets are the preferred method of pick up. Do not make contact directly with the die surface as this will damage the monolithic circuitry. Air bridges must be avoided during placement. Handle with care.

RF connections should be made as short as possible to reduce the inductive effect of the bond wire. Use of a 25 µm thermosonic wedge bonding is highly recommended as the loop height will be minimized. Force, time, and ultrasonic are critical parameters.

RoHS Compliance

The product is compliant with the 2011/65/EU RoHS directive 2015/863/EU and REACH N° 1907/2006.

Contact Information

For additional technical Information and Requirements: **contact.mec@mec-mmic.com**

Notice

The furbished information is believed to be reliable. However, performances and specifications contained herein are based on preliminary characterizations and then susceptible to possible variations. On the basis of customer requirements, the product can be tested and characterized in specific operating conditions and, if needed, tuned to meet custom specifications.